Patrick Moorhead: Hi, this is Pat Moorhead. Welcome back to The Six Five Summit day two. We are talking about one of my favorite topics, semiconductors, maybe it's my favorite topic, and we are diving deep on some important technology that Intel is delivering, not only to its internal design teams, but also to its IFS customers. With that, I'd love to welcome Ben and Eric. Welcome, first time Six Five.

Ben Sell: Thanks, Pat. Great to be with you today.

Eric Fetzer: Nice to meet you, Pat.

Patrick Moorhead: We've had some awesome Intel folks here on either The Six Five podcast, The Six Five Summits, heck, we even had Pat G, who he refers to me as Little Pat and I refer to him as Big Pat, who kicked off the Summit a few years back, and I'm ready to talk about some incredible semiconductor technology. Maybe a great place to start, maybe Ben, you can kick this off. Talk about what you do for the company and then Eric, you can go afterwards.

Ben Sell: All right. Thanks, Pat. Yeah, I'm vice president for technology development at Intel, responsible for our technology programs. We have our technology roadmap and I'm responsible to make sure that the different programs stay on track and we can deliver the future.

Patrick Moorhead: Future is good. Future is important.

Eric Fetzer: I'm Eric. I'm an Intel fellow. I work in the design organization to align the technologies that Ben delivers and figure out how we take that technology and develop our next generation products.

Patrick Moorhead: I love that. Many times people forget just how long it takes to create a design, take it into manufacturing, but by the way everybody's working on all the transistors and all the fab technologies along the way, it truly is impressive. Why don't we start, Ben, with you? One of the big technologies that Intel has been talking about is this concept of backside power delivery. Can you talk about why this is important and how this relates to Moore's law?

Ben Sell: Yes, of course. The way we build our chips is we start with the tiniest features, the transistors, then layer by layer, we add wiring to it from tiny wires to slightly less tiny wires. Currently, these wires fulfill two applications. One is we have the signal wires that connect the transistors with each other and within dye connection and we have the power wires that connect the power supply to the transistors themselves.

As we scale down the size of the transistors, the wires also have to get smaller and smaller and over time become more and more a bottleneck for the performance and the scaling of the transistors. What backside power delivery is doing is it's taking the power wires from the front side and putting them on the backside of the wafer. This gives us a lot more room for the front side wires to be bigger, while still enabling the scaling of the transistors, giving us a lot more performance, and the power delivery is a lot more direct to the transistors giving us higher performance, in addition.

Patrick Moorhead: Yeah, that's great. Eric, what does this mean to the chip? And we've talked about the technology, the backside power delivery, separating the power from the signal, but what does that mean for the chip, the power or the density and the performance?

Eric Fetzer: First of all, the backside metal gives us the best possible power delivery scenario we can have on chip, and those losses are substantial. By eliminating those losses, we get lower power and higher frequency. The second aspect of it is by removing the power from the front side metals, Ben mentioned we get bigger interconnects. Well, we can use those bigger interconnects to improve our frequency, to reduce our switching capacitance, which is save power, and enable smaller area all at the same time. To put a little quantitative data into it, we were able to rebuild our core with this technology and get 90% cell utilization, a 30% reduction in power supply losses, and almost a 6% frequency improvement just from a rebuild with no other changes.

Patrick Moorhead: I love it when you guys talk like that. There are other ways to do backside power. I do a lot of research on Intel, but I do a lot of research on the industry itself. I'm curious, this is probably a question for Ben. How does PowerVia Intel's PowerVia approach, how's it different from other ways that people are approaching this and why is it better?

Ben Sell: Yeah. Intel's PowerVia is a direct connection to the contact of the transistor from the backside. This gives us a very low resistance path from the bumps to the transistors themselves and further improving performance, but it also does not go through the lower metal layers like some of the other backside power delivery solutions that are out there. And what this does is it frees up the lower metal layers and does not consume any wiring for power delivery. And as Eric mentioned, this allows us to widen the pitch of the lower backend layers. With this one, we can achieve multiple things. First of all, we get better performance because we have fatter wires and can deliver the signals better, but it also reduces the requirement for very aggressive scaling of those layers. The scaling of those layers, first of all, it's very expensive and the cost we are saving from not being that aggressive more than offsets the cost for actually doing the entire backside power delivery process. In addition, less scaling also means it's the most stable process and has less risk for yield.

Patrick Moorhead: No, that's good. Having been in and around semiconductors for over 30 years, and it's funny. I was a specker and a buyer of semiconductors for an OEM, worked for a semiconductor company for a long time, and here I am, last 12 years being an analyst to the semiconductor industry. It really all comes down to delivering PPW for certain workloads and I think as the industry has progressed, there's been more of a focus on specific use case. I'll direct this question to you, Eric. Are there any specific applications, workloads, use cases, where backside power delivery really shows its true colors?

Eric Fetzer: Sure, Pat. With backside power delivery, one of the key things is it delivers performance improvement across all the workloads, but specifically the ones that take high power, the ones that drive changes in power consumption in the part. Those would be things like AI, graphics, high performance computing, and even gaming. Those workloads in particular, the backside power truly shines.

Patrick Moorhead: That's awesome, and by the way, that's where the ball's headed. There's no doubt in all the research that we do and it's not just the conversation and the big fireworks that are going out. This is where we need this type of enablement. Ben, I understand that you've created a very special node and a test chip for PowerVia to validate all these performance expectations for the workloads that Eric talked about, and I hear you're doing very, very well. And by the way, if I track you on nothing else, it's five nodes in four years. Can you tell us more about the test that you're exceeding expectations on and maybe talk about some of the results and the metrics that you're basing that off of?

Ben Sell: Yes, of course. When you look forward, the fourth and fifth node, we are delivering Intel 20A, Intel 18A. Those nodes, we have two big innovations we are putting in: PowerVia and RibbonFET. One thing we wanted to make sure is that we understand and debug the PowerVia process ahead of RibbonFET, so that we don't have two big problems to solve at the same time. We created a node, where we took our Intel 4 Process and added PowerVia on top. And there were four main items we wanted to get out of this test chip and our product like test chip as well.

First, we wanted to make sure we developed the process, get good yield, get good reliability, understand whether there are any shifts in device per metrics and fix those, so that one we have done successfully with our test chip. Second, as soon as you put backside metals on the chip, it does change your abilities to do chip level debug, since many of the techniques required to have access from one side. With this test chip, we could validate the new technologies for debug that we have to developed and validate that the working and that we can find design bugs and also process defects. The next item that we wanted to make sure is that we understand the thermals. As soon as you also put wires from both sides of the transistor, we wanted to make sure that the models we have for how thermals behave are accurate and that we can develop and test solutions to address any concerns with thermals, and that also we have done and we have now developed solutions that we can give our customers to deal with the thermals on backside power delivery process.

Patrick Moorhead: A lot of these decisions are all about risk and de-risking PowerVia from 20 Angstrom seems like a good idea, but why would we want to combine the two and maybe just not offer them further down the road? Maybe this is an obvious answer, but I have to ask, Ben.

Ben Sell: Yes. No, this is good. The fourth item from the list I just mentioned is we wanted to make sure we can demonstrate the intrinsic value proposition of PowerVia. Overall, when you look at it-

Patrick Moorhead: Separated, in a way.

Ben Sell: Yeah. If you look at it, both the PowerVia and the RibbonFET provide a significant value proposition that we want to give to our customers as soon as possible. Currently both of these look very good in our development lines and we wanted to make sure that we can de-risk those and make sure both of them are ready, but give both of them to our customers as soon as we can. And overall, what we are seeing is whenever we have a new node, there's a lot of new development, a lot of new IP that we need to develop. We wanted to make sure that our design

partners have the full package so that the design and Rp1s can use it for all our Intel 20A and Intel 18A products.

Patrick Moorhead: No, that's good. I get it now. Thank you. It really does take a village and with Intel supporting industry standard EDA tools out there that translates to having to support special valuable features like backside power. What do the architects, the chip designers out there need to know about it? Is the industry ready? Is it there? Where are we on this map. Maybe Eric, that's for you,

Eric Fetzer: Sure. We have full, what I'll call basic EDA support from the large vendors today. By no means have we hit the point where it's delivering the absolute best, so we're still working with the vendors to improve the performance of the results and the capability of the results. And in a few places, we rely on design methodologies to cover the holes. In the future where we expect tool and EDA vendor optimizations to help us out potentially, in things like signal shielding and thermals that Ben had mentioned, there are some opportunities still, but with the packages we have today, we're able to leverage the core value of backside metal and PowerVia with the vendor support we have today.

Patrick Moorhead: I think that's good news. And by the way, I give Intel a lot of credit for the increased supportive industry standard tools. I can tell you from experience, it took a lot. It takes many years to shift to that and you have to, particularly when you want to be a leading foundry, which I know IFS wants to be, to other companies that might be using different tools. Let's talk, Eric, another question for you. From an IFS business, so an Intel foundry business perspective, what is the potential and business potential competitive landscape for PowerVia? I know it's got to be hard to put that all on one feature, but it does seem like it is one of the bigger differentiators that obviously internal Intel designs could take advantage of, but as importantly, or even more importantly, IFS customers.

Eric Fetzer: Right. When we look at a feature like PowerVia, first of all, why are customers buying the technology in the first place? It comes down to performance, power consumption, and area, and PowerVia really addresses all three of those areas very directly. We get significant improvements in our ability to deliver power and power consumption, we get the frequency improvements that we discussed, and we also are getting significant improvements in areas. This leaves us a node ahead from the results of PowerVia versus what competition is offering in the same space. From a customer perspective, it's delivering on point for what they're looking for. Combined with the EDA support, we can deliver a package that enables them to bring this to market with their designs in a quick and efficient manner.

Patrick Moorhead: I love it. Isn't it funny after 40 or 50 years in this industry, it's PPA, always been. Started off with PPA and it's still PPA. We might be doing it differently. We might be measuring a little differently. It might be more systemic than at the micronic or subatomic, but it's still all about PPA. I love that. What's old is new. What's new is old.

Gentlemen, I've really enjoyed this conversation, but I wanted to hit you up with one final question here. Does backside power and Gate-All-Around show that Moore's law isn't dead? And listen, I've been hearing about the death of Moore's law forever, but I wanted to make sure

you're able to weigh in. And my corollary to that is, what are you thinking beyond these new transistor innovations? And Ben, why don't we start off with you?

Ben Sell: Yes. Moore's law is alive and well. The two innovations that we have, PowerVia and RibbonFET, which is our version of Gate-All-Around, are a critical inflection point for our aggressive five nodes in four years roadmap and getting back to process leadership by 2025.

Eric Fetzer: From my perspective, these are two steps in an ecosystem to get me to a trillion FETs in a package. We're looking at 3D constructions, disaggregation, technology optimizations for functions, including memory and power delivery, much like what PowerVia and backside metal provide. This is a step on the journey to get there and we see a good roadmap going forward of technologies like these to get there.

Ben Sell: Yeah, and coming back to the roadmap that Eric just mentioned, first of all, RibbonFET and PowerVia, the innovations we have from that, that will carry us for the next two process node at least. And then we have many very interesting options in our labs we are testing, like CFET or new channel materials, that propel us further going from there.

Eric Fetzer: Well, it's our job to leverage the technology that Ben delivers now and into the future, and we're doing that through several methods, including taking the new technologies and combining them with old technologies or specialized technologies. One of the things I'll highlight is specialization, whether it's memory, power delivery, those kinds of things are becoming a larger role and Ben is enabling these features for us. Each generation, something new is being added, particularly with PowerVia, it's a power delivery technology, but he's going to give us more magic in the future.

Patrick Moorhead: That's what we need, just more magic to get us forward here, and it is so funny. I'm just always astounded at the amount of research, the amount of engineering hours that go into making this happen. And listen, every decade I hear that, "Oh, we've hit a wall," but somehow the industry, through sheer brilliance, a tremendous amount of investment, keeps moving it forward because the industry success and quite frankly, Intel's success is paramount to the future of all of these innovations.

I, for one, love to see all the competitive foundry capabilities brought to the table. I'm not confused at how much investment that takes, how different that takes to be able to serve different types of customers for IFS. Obviously, just to serve a really big, IFS customer, the internal Intel design teams happens to be an important one as well, so it's good to see Intel bringing out some very demonstrable and differentiated technologies. I've been aware of PowerVia, I think, going on four to five years now, and that's just how long ... I mean, you didn't even just start this, though. You started a lot longer and it's almost like a miracle that some of these technologies come to the table.

Ben and Eric, I just want to thank you again for coming on The Six Five Summit 2023 day two and really making this program more exciting. You know I love semiconductors, our audience loves semiconductors, and we love doing the double click learning about new technologies like backside power through Intel PowerVia, so thanks again for coming on.

Ben Sell: Yeah, and thanks for having us, Pat. It was great to talk to you about PowerVia and what the future brings.

Eric Fetzer: Yes, Pat, it was an absolute pleasure.

Patrick Moorhead: Love to have you back on to learn more about it, maybe even do a victory lap as we get closer to full production.

Eric Fetzer: Sounds like a great plan.

Patrick Moorhead: I want to thank everybody for tuning into this segment of The Six Five Summit day two semiconductors, and we are just absolutely doing a double click on cool technology, backside power delivered by PowerVia and Intel. We are hopeful as an industry that it will deliver tremendous benefit to not only Intel semiconductors, but also its IFS customers. Stick around, we're going to be talking a lot more semiconductors here in day two. If you missed day one, it's okay. It's on record. It's on time lapse. Go back and check it out and also check out day three, because we're going to be interviewing companies that are the most relevant in the technology industry and their executives. Take care. Thanks again.